Dr. Hardik Shah

Experience

12.2012 - present **Staff researcher**, Robotics and Embedded Systems, Technical University Munich, Germany.
Research in the area of multi-core architecture for safety critical hard real-time systems. Development of innovative low level micro-architectural components (caches, arbiters) to achieve predicable execution time at low performance penalty (Demonstration).

Detailed achievements

- Supported Airbus in analyzing new multi-core technology from a start-up.
- Established co-operation with Altera to get in the *Early Access Program* for OpenCL.
- Supervised several bachelor and master theses.
- Organized a highly popular lab course on Model Autonomous Cars.
- Trained and supervised the 2015 Audi-autonomous-cup **winning team** (MomenTUM).
- Monitoring several experiments in the FP7 funded Echord++ project.

09.2012 - present **Visiting trainer**, SYSU, Zhuhai, China.
Training more than 450 Chinese engineering students on Model Autonomous Cars.

03.2015 - 02.2016 **StartUp** - **Autca**, Munich, Germany.
A low cost and low maintenance educational autonomous car for Universities and students.

Capabilities and specifications

- Lane detection and following, Autonomous parking, ESP, Obstacle avoidance, Video feedback on a mobile App, WLAN connectivity.
- 3-core architecture on a low cost FPGA board, μC OS II RTOS, C/C++ programmable.
- 1x VGA camera, 3x gyro/accelerometer, 3x compass, 8x ultrasonic sensors, 4x motors, 4x wheel encoders, 1x WiFi Module, 2x head/tail lights, 4x blinkers.
- Online courses on: C/C++, embedded systems, lane detection etc.

01.2010 - 12.2012 **Staff researcher**, ForTISS GmbH, Munich, Germany.
Development of innovative low level micro-architectural components (caches, arbiters) to achieve predicable execution time at low performance penalty (Demonstration).

Detailed achievements

- Invented a shared resource arbitration scheme for significant performance improvement and predictable execution time.
- Written research proposal and acquired funding for the TU9 project.
- Built demonstrators for promotion events – Embedded world '10/12, Open house day.

Hamburger Strasse 40 – 80807 Munich
+49 17696487171 • shah@in.tum.de • www6.in.tum.de/Main/Shah

05.2008 - 03.2009 **Digital Design Engineer**, TES Electronics Solutions GmbH, Düsseldorf, Germany.
Functional verification of TOSHIBA processor components. Test case development of PortMux, UART, I^2C, CCR etc components.

Detailed achievements

- Automated a recurring two person month consuming verification task.

10.2006 - 05.2008 **Hardware/Software Engineer**, NERO AG, Karlsbad, Germany.
Development and optimization of digital Hardware and software modules.

Detailed achievements

- Achieved significant savings in chip area and increase in operating frequency by porting hard-coded FSM of an AAC bit-stream parser to a 4 stage pipelined processor with customized instruction set architecture.
- Optimized Dolby and DTS audio codec to achieve three times faster execution.

08.2005 - 06.2006 **Master thesis**, IHP Microelectronics GmbH, Frankfurt (Oder), Germany.
Design and development of IEEE 802.1.3 MAC protocol accelerator.

Detailed achievements

- Achieved 13 times faster execution by accelerating critical tasks in hardware.

Education

01.2010 - 12.2015 **PhD**, Technical University Munich, Germany.
Thesis: "Predictable and high performance Multi-core Architectures"

09.2004 - 06.2006 **Master of Science**, KTH, Stockholm, Sweden.
Electrical Engineering, Specialization: "System on Chip"

09.1999 - 06.2003 **Bachelor of Engineering**, South Gujarat University, Surat, India.
Electronics and Communication Engineering

Publications

A link to the Google scholar page

Skill Summary

Programming	VHDL, C, MISRA-C, SystemC, TLM2, Verilog, C++, TCL, Intel SIMD instructions, ARM Assembly, 8051 Assembly, 8085 Assembly
Tools	Modelsim, Altera Quartus, NIOS II SBT for Eclipse, KiCAD, Microsoft Visual Studio, Xilinx ISE, Synopsys Design Analyzer, Intel vTune, Cadence NCVerilog
Management	SVN, Git, CVS, Redmine, Producteev, GanttProject, Perforce
OS	MS Windows, Ubuntu Linux

Personal Details

Nationality	Indian
Work permit	Daueraufenthalt EG (Allowed to permanently work in majority of EU countries)
D.O.B	17^{th} November 1981
Languages	Gujarati, English, Hindi, German (B1)
Hobbies	Volleyball, Cricket, Traveling, Cars, Robots