

Evaluation of a Multi-Core Architecture for a Quadcopter Control Application



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Background

Multi-core / many-core architectures are increasingly used in the domain of embedded systems to exploit the advantages of these systems over conventional processors, e.g. lower power consumption. The propeller chip was designed especially for the domain of embedded systems and has unique features such as deterministic latencies for cache access.

Description

The goal of this project is to set up a working toolchain for the propeller chip and to evaluate its general applicability using a set of sample applications. In the later course of the project, the student will integrate the propeller chip using her/his implementation into the quadcopter project that is currently performed at the fortiss research labs.

Tasks

In the course of this student project, the following items will be dealt with:

- Setup of the development toolchain.
- Definition and implementation of sample applications.
- Integration of I/O devices (analog/digital input/output) to use the chip in the quadcopter project.

References

- [Propeller chip](#)
- [fortiss](#)

Supervisor:

Prof. Dr.-Ing. Alois Knoll

Advisor:

Dipl.-Inf. Simon Barner

Research project:

Type:

BA, SEP

Research area:

Embedded Systems,
Parallelization

Programming language:

C, C++

Required skills:

Low-level programming,
Electronics, basic knowledge
about control theory

Language:

English, German

Date of submission:

13. November 2009

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