

Evaluation of the Cell Processor Architecture

Background

The Cell processor basically consists of four components

- external input and output structures
- Main processor: Power Processing Element (PPE), based on PowerPCMain processor
- 8 Co-processors: Synergistic Processing Elements (SPEs)
- Highspeed bus: Element Interconnect Bus (EIB)

Computationally intensive tasks can be computed in parallel by the PPE and the SPEs that can exchange data with main memory or external data storage using DMA (direct memory access). Since a SPE's load/store operations can only access local memory, they entirely rely on DMA to send or receive data.

Description

The goal of this project is to set up a working toolchain for the propeller chip and to evaluate its general applicability using a set of sample applications.

Tasks

In the course of this student project, the following items will be dealt with:

- Setup of IBM's development toolchain on a Playstation 3 (see below)
- Definition suitable benchmark applications and implementation of a demonstrator

If the project is to be performed as a MA or DA, additional emphasis will be put on conceptual / theoretical aspects such as the evaluation of existing software development approaches for the Cell architecture.

References

- [Programming high-performance applications on the Cell BE processor. An introduction to Linux on the PLAYSTATION 3](#)
- [An Open Source Environment for Cell Broadband Engine System Software](#)
- [A new record for the elliptic curve discrete logarithm problem \(ECDLP\) using PS/3](#)



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Research project:
EasyKit

Type:
BA, SEP, MA, DA

Research area:
Embedded Systems,
Parallelization

Programming language:
C, C++

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Parallel programming,
Electronics

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English, German

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