

Master/Bachelor thesis proposal

Using FPGA to implement computer vision applications

1 Introduction

Typically, computer vision applications are processed using high performance accelerators equipped with huge computation power so as to meet the real-time demands. Most of the existing works use graphic processing units (GPUs) as their acceleration platforms. However in the near future, with the widespread use of these applications in mobile and automotive area, it's inevitable to transplant them on the low-power-cost, portable and embedded processing units like FPGAs.



Figure 1: A sketch map of modern computer vision algorithms, which need high computing power

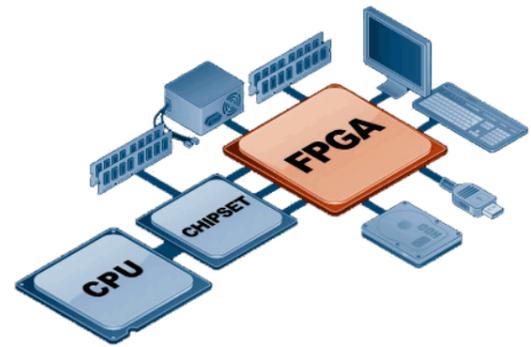


Figure 2: FPGA as an accelerator in the system

FPGA is a type of high performance and low power cost device that is very suitable for data acquisition and processing. Compared with GPUs, FPGA is able to be reconfigured with processing units and customized memory hierarchies. Besides, the power cost is also much lower. Currently there exists some work that attempts to using FPGA to perform the real-time image processing applications. Nevertheless, these efforts are still very preliminary.

2 Motivation and Goals

We want to implement the classic digital image processing algorithms on the FPGA, using the high-level synthesis (HLS) methodology. By using FPGA, we want to observe to which extent the computation and real-time performance can be. Moreover, based on this framework, we could further impose it on more advanced computer vision applications.

3 Your tasks

- Understand the basic principle of the classic digital image processing algorithms.
- Port the software-like algorithm into the hardware-like module design on the FPGA.
- Optimize the design to get real-time performance.

4 Requires

- Basic knowledge on programming and algorithm design
- Very good knowledge on FPGA hardware design

5 Contact

Xiebing Wang
Institut für Informatik VI, TUM
Room MI 03.07.059
wangxie@in.tum.de
+49.89.289.18128

Biao Hu
Institut für Informatik VI, TUM
Room MI 03.07.042
hub@in.tum.de
+49.89.289.18111

Kai Huang
Institut für Informatik VI, TUM
Room MI 03.07.042
kai.huang@in.tum.de
+49.89.289.18111